COMPUTER-AIDED DESIGN OF CLASS-C MICROWAVE TRANSISTOR AMPLIFIERS BY DIRECT NUMERICAL OPTIMIZATION

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ABSTRACT

In this paper we outline a straightforward procedure for microwave class-C amplifier design. We first discuss an empirical bipolar junction transistor model of an enhanced Ebers-Moll type, allowing an accurate simulation of the device performance in the power saturation region. We then describe the use of this model in conjunction with a general-purpose harmonic-balance simulator, to provide a direct numerical optimization capability for the class-C amplifier. Finally, as an illustrative example, we report on the simulation of a practical MIC amplifier built on teflon-fiberglass substrate.

INTRODUCTION

The design of class-C transistor amplifiers still represents a challenge for the microwave engineer. Although some work on the computer-aided simulation of this kind of circuit has been reported in the technical literature {1}, there is a definite lack of a straightforward CAD solution to the amplifier design problem. Even modern textbooks {e.g., 2} suggest design approaches based on standard empirical techniques such as the load-pull method, supported by previous experience and by elementary rule-of-thumb calculations.

An obvious prerequisite for the development of a systematic CAD procedure is the availability of a bipolar junction transistor (BJT) model providing adequate description of the device behavior (especially of its power saturation mechanism) at high drive levels. This model should be coupled with a state-of-the-art harmonic-balance simulator with optimization capabilities {e.g., 3} to provide the necessary CAD tools. In this paper we start from a classic BJT model of a modified Ebers-Moll type {4} and first discuss the model enhancements required to allow an accurate prediction of the saturated output power and of the associated values of collector efficiency and power gain. We then outline a straightforward design approach based on numerical optimization, allowing the determination of a realistic amplifier topology fulfilling a set of specifications on output power, collector efficiency, transducer gain, input match, and stability margin. The effects of all significant harmonics of the source frequency (usually 6 to 8) are exactly taken into account during the optimization, and the final design can be checked for low-frequency and parametric instabilities. The details of a practical MIC design are presented as a validity check for the numerical method.

The approach described herein could represent a powerful support for the amplifier designer by providing an attractive alternative to the traditional methods based on empirical load-pull contouring.

DETAILS OF BJT MODEL

The BJT model adopted is an Ebers-Moll equivalent circuit having the topology shown in fig. 1 for the intrinsic device. This has been preferred to an integral charge-control model because of its higher numerical efficiency {4}, which is essential for optimization purposes. Basic requirements for large-signal simulation are that the base push-out effect, the conductivity modulation in the base region, and the collector breakdown are taken into account. Thus the following modifications are introduced with respect to a conventional Ebers-Moll model: i) the common-emitter current gain β_F in the active region is described as a function of the injected current i_F by a polynomial approximation {5}; ii) the intrinsic base resistance is modeled as a decreasing function of i_F {4}; iii) the emitter diffusion capacitance is represented as a polynomial function of i_F {4}; iv) the avalanche multiplication in the collector depletion layer is accounted for by classic empirical models {6}. When it comes to the analysis of a class-C amplifier operated in the power saturation region, this is still insufficient, since additional effects become of importance in the presence of very large voltage and current swings. The necessary enhancements with respect to the above-described model include at least the following aspects:

1) the current gain fall-off at high injection levels;

2) the dependence of collector current in the active region on collector voltage (Early effect);

3) the current gain drop in the quasi-saturation region in the common case of n^+-p-v-n^+ (or similar) devices.

The models adopted are briefly described below. In all cases they are based on available bipolar transistor theory, but are suitably parametrized in order to allow a good empirical fit to the observed behavior of the device in use.

1) The polynomial approximation adopted for the current gain can accurately represent β_F in a given

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current range, say $[i_{F1}, i_{F2}]$ where experimental information is available (e.g., from the collector characteristics). However, in order to accurately evaluate the saturated output power, the asymptotic behavior of β_F for large current values is also important. An empirical relationship adequate for simulation purposes is

$$\beta_F = \beta_{F2}\left(\frac{i_{F2}}{i_F}\right)^p \qquad (1)$$

where $i_F > i_{F2}$ and β_{F2} is the value of the polynomial expression at i_{F2}. Two important theoretical limiting values of the exponent p are $p = 1$ in the absence of emitter crowding, and $p = 2$ in heavily crowded conditions {7}. In practice p is empirically established in relation with the saturated output power of the particular device in use. Note that p values larger than 2 were experimentally reported in some cases {7}.

2) When the collector voltage swing is large (several tens of volts or more) the existence of a nonzero collector differential conductance (Early effect) may become important, and cannot be neglected. As it is well known {7}, the Early effect results in a positive slope of the collector DC characteristics in the active region. This slope is an increasing function of current, in such a way that all the I-V lines intersect the negative voltage axis at approximately one point (i.e., at the so-called Early voltage). In order to empirically model this phenomenon, in the active region the forward current gain β_F (depending on i_F only, as previously mentioned) is replaced by

$$\beta_{FE} = \beta_F\left[1 + \frac{v_{CE}}{(\beta_F+1)V_A}\right] \qquad (2)$$

where V_A is an empirical parameter proportional to the Early voltage. According to (2) the slope of a collector characteristic in the active region is $\beta_F i_B/[(\beta_F+1)V_A]$, and is thus an increasing function of i_B even in the region where a gain drop is observed. Eq. (2) was found to provide an excellent fit to the measured I-V curves, an example being given in fig. 2.

3) A high-voltage power BJT usually has an n^+-p-ν-n^+ or similar structure, rather than a simple n-p-n one. At relatively low collector voltages, when the collector current becomes large enough so that the voltage drop across the ν region exceeds the applied v_{CB}, the collector junction becomes forward-biased and the base width increases {8}. In this "quasi-saturation" region the current gain for a given i_F is lower than in the active region. This results in a stronger voltage- and current-limiting effect and in a significant reduction of the saturated output power.

In order to properly account for the quasi-saturation effect, a nonlinear series resistance (representing the ν region) should be introduced in the equivalent circuit at point B' (fig. 1). To avoid this difficulty, we simply update the current gain value, after {8}, by the equation

$$\beta_{FQS} = \beta_{FE}\left[1 + K_\nu v_{CE}\left(\frac{v_{CE}}{R_\nu i_C} + \frac{R_\nu i_C}{v_{CE}} - 2\right)\right]^{-1} \qquad (3)$$

where K_ν and R_ν are empirical parameters, the latter representing the series resistance of the unmodulated ν region. β_{FE} is replaced by β_{FQS} throughout the quasi-saturation region, i.e. for $i_C > v_{CE}/R_\nu$. This approach is phenomenological, and does not account for the forward biasing of the collector junction in the quasi-saturation region; however, it can be used in general to effectively model a current gain drop occurring at low collector voltages. Note that in {9} a different model of the quasi-saturation region was proposed, which is much more complicated, but theoretically more accurate than (3). Nevertheless, (3) was preferred because it produces satisfactory results after properly adjusting the empirical parameters K_ν, R_ν.

Fig. 2 shows that our model can fit the measured collector DC characteristics of a practical device (MSC 3000) with acceptable accuracy.

In order to formulate the dynamic device equations, we make use of the state-variable approach described in {10}. If the junction voltages v_{BE}, v_{BC} (see fig. 1) are chosen as the state variables, the equations can be written down by inspection of fig. 1, despite of the presence of the nonlinear base resistance R_B. The result is a powerful simulation tool coupling unmatched modeling accuracy with high numerical efficiency.

CIRCUIT OPTIMIZATION

We now outline a general optimization procedure for a class-C amplifier and describe its application to a practical design problem. The specifications for the latter are an output power $P_{out} \geq 650$ mW, a collector efficiency $\eta_C \geq 35\%$, a transducer gain $G_T \geq 8$ dB, and an input return loss $L_{Rin} \geq 13$ dB at 2.25 GHz. The transistor in use is a packaged common-base MSC 3000 device. The device and the package are modeled on the basis of DC and RF measurements. The device model refers to the actual operating temperature, which can be roughly evaluated a priori making use of the known thermal resistance.

As it is commonplace in circuit optimization problems, a suitable topology is first selected. For the design example under consideration, this consists of a two-section transmission-line transformer on the output which can load the collector with any required low impedance (both lengths and impedances are variable), and a single-stub matching section at the input (emitter). The collector bias supply is kept fixed at $V_{CC} = 28$ V; a resistor R is introduced in the emitter DC circuit in order to self-bias the emitter junction to a negative voltage, thus decreasing the conduction angle and increasing η_C {2}.

A good optimization approach is to decouple the input and output circuit design, since this results in a

much better-conditioned numerical problem. For this purpose the input matching network is suppressed during a first design stage, and the available power of the RF source (P_A) is treated as an additional optimization variable. Despite of this, the information on the effects of input matching is not lost. In fact, if we introduce the power-added efficiency η_A, the power flowing into the circuit at the input port is given by

$$P_{in} = \frac{\eta_C - \eta_A}{\eta_C} P_{out} \qquad (4)$$

so that the transducer gain in matched-input conditions can be expressed as $G_{Mi}=P_{out}/P_{in}$. Thus the first optimization is run with the given specifications on P_{out} and η_C, no specification on L_{Rin}, and the original specification on G_T transferred on G_{Mi}. The design variables are the output circuit parameters, P_A, and the self-bias resistance R.

It turns out that this kind of optimization has a definite trend towards circuit instability. This means that the numerical algorithm almost invariably leads to a load impedance for which the input impedance has a negative real part. It is not difficult to understand why this is so: from a purely numerical viewpoint, instability is a very happy condition whereby the gain becomes infinite, and in general all specifications are most easily satisfied. In order to avoid this, we only have to impose the condition $P_{in} > 0$, or $\eta_C > \eta_A$. Under this respect, the quantity $\eta_C - \eta_A$ can be viewed as a stability margin. Thus the first optimization is actually run with the addition of an *upper* bound on the power-added efficiency (typically, η_C - 5%).

Once the output transformer and the bias resistance have been found as described above, the input matching section is reintroduced together with the specification on L_{Rin}, and a second optimization step is run. In this case the optimization variables are the input circuit parameters and the available RF power P_A. This yields the final circuit configuration and the required RF source.

Figs. 3 and 4 show the good agreement obtained between the expected and measured performance of the amplifier, which was built on DUROID substrate by hybrid techniques. Note that the predicted output power is slightly in excess (about 50 mW) at low input power levels right after the amplifier turnon. This is probably due to the imperfect simulation of the current gain drop at low collector voltages (which is very critical) provided by the model (3) (see fig. 2). For comparison, we also report in fig. 3 the P_{in}-P_{out} curve obtained when this effect is completely neglected (K_v=0 in (3)): in this case the output power is strongly overestimated across the entire input power range. Note that the shapes of the experimental curves, which are typical of the class-C amplifier (see {11} as a further reference), are accurately reproduced by the present simulation. This is not the case for less refined BJT models whereby the above-mentioned large-signal effects are not accounted for.

The above method fulfills a condition which is necessary, but not sufficient, for the amplifier stability. Since this is a critical issue, the procedure must be completed by checking the final design for DC and parametric instabilities. To do so, we first parametrize the circuit by the collector bias voltage in the absence of RF drive, and search for Hopf bifurcations of the DC operating point in the range [0, V_{CC}]. Then, with the collector bias kept constant at V_{CC}, the circuit is parametrized by the RF source power (ranging from 0 to the nominal value), and the solution path is searched for period-doubling and Hopf bifurcations. If no bifurcations are found, the amplifier is stable {12}.

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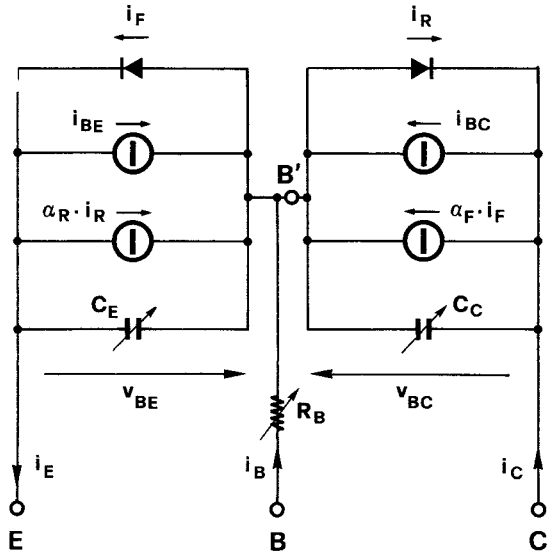

Fig. 1
Nonlinear equivalent circuit of a bipolar junction transistor.

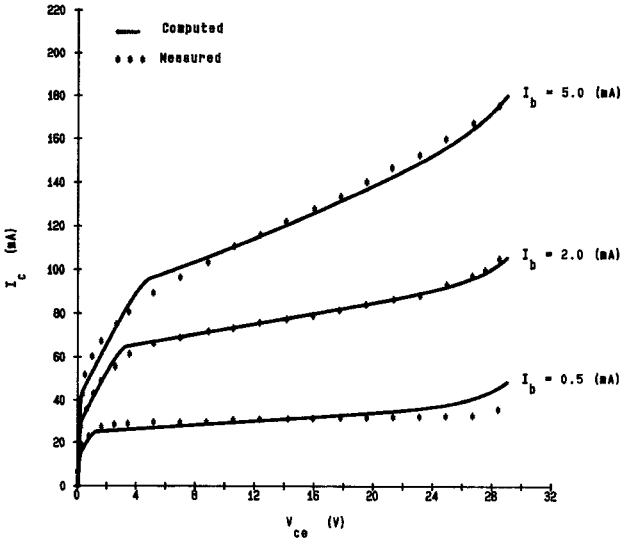

Fig. 2
Simulated and measured collector characteristics of a BJT.

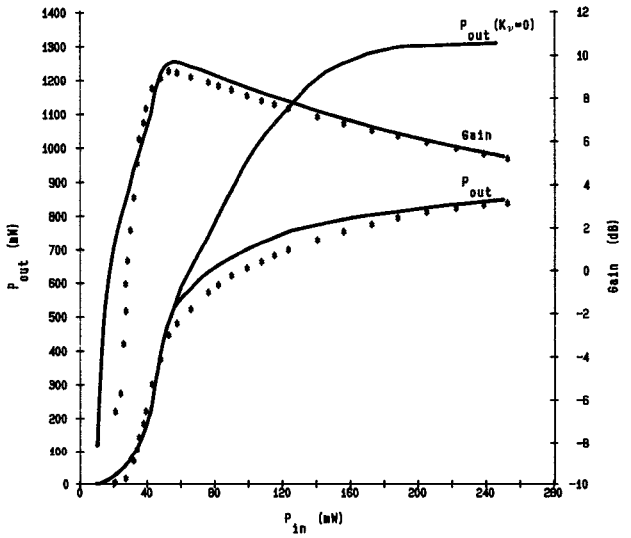

Fig. 3

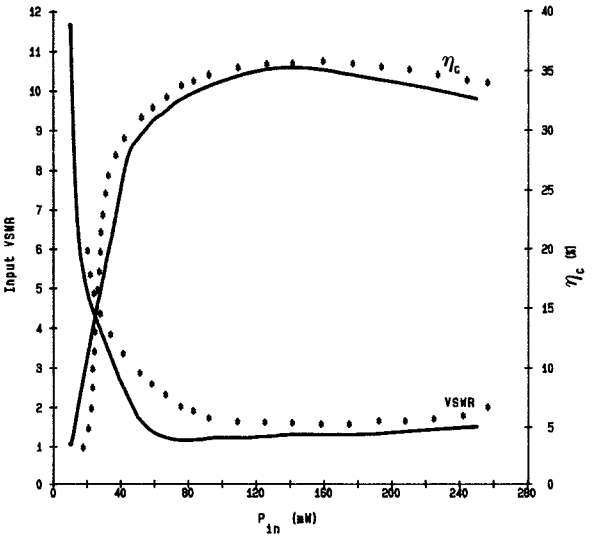

Fig. 4
Simulated and measured performance of a hybrid class-C BJT amplifier.